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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,657	01/20/2004	Chin-Kun Fang	67,200-1176	3412

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EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,657	FANG ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 33-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,20 and 33-40* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed February 10, 2006.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-18, 20 and 33-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama et al. (US 6,603,162) in view of Yu (US 5,911,110) and Applicant's admitted prior art.

Regarding claim 1, Uchiyama discloses providing a process wafer, forming a nitride mask over the wafer, providing the wafer and mask with active area (CR) trenches and at least one inactive area (DR) trench, forming a filling layer (6) over the active area trenches and the inactive area trenches to substantially fill the trenches, and planarizing the wafer process surface such that the active area trenches and the inactive area trenches are substantially coplanar (Fig. 8(a)-10(b); col. 9, ln. 31 – col. 10, ln. 8).

Uchiyama does not disclose forming a patterned resist layer between the active and inactive trenches and removing the filling layer not covered by the resist layer. Like Uchiyama, Yu discloses forming isolation trenches in a semiconductor substrate, wherein isolation filling material is deposited into the trenches and then planarized to form coplanar trenches. Yu teaches that when using a planarization method such as that of Uchiyama, the trenches are subjected to undesirable dishing and erosion of the nitride mask layer (col. 1, ln. 31-53). To avoid the problems with the planarization method used by Uchiyama and the conventional prior art, Yu suggests forming a resist layer including patterned portions disposed between the trenches and

removing the filling layer portions not covered by the resist layer (col. 4, ln. 15-37). By this method, Yu discloses that the etching rate of all areas of the filling layer can be made uniform, thus preventing the dishing and nitride mask erosion problems of the prior art. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method of Yu, including the steps of forming a resist layer including patterned portions disposed between the trenches and removing the filling layer portions not covered by the resist layer, in the isolation planarization process of Uchiyama because Yu teaches that this method can successfully prevent the dishing and mask erosion problems inherent in the prior art.

Uchiyama does not disclose that the inactive area trenches overlie a laser-marked portion. Applicant's admitted prior art discloses that it is conventional in the art to form a laser-marked identification mark on the periphery of a wafer so as to be able to track the wafer throughout the various processing steps that it will undergo (paragraph 002). At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide a laser-marked identification mark at the inactive peripheral area of the wafer of Uchiyama in order to be able to track each particular wafer through its processing steps.

Regarding claims 2, 34 and 38, Uchiyama discloses that the planarization process is a CMP process (col. 10, ln. 4-8).

Regarding claims 3, 35 and 39, Yu discloses that the step of removing the filling layer portion is conducted by a plasma (dry) etching process (col. 5, ln. 4-5).

Regarding claims 4 and 12, the admitted prior art discloses that the laser-marked identification mark is conventionally forming in an exclusion area at the process wafer periphery adjacent the process wafer peripheral edge (paragraph 002).

Regarding claim 5, Uchiyama discloses that the active area trenches are shallow trench isolation trenches (col. 1, ln. 28-39; col. 8, ln. 23-40).

Regarding claims 6 and 13, Uchiyama discloses that the process wafer is a silicon substrate and has an overlying nitride layer (col. 9, ln. 17-30).

Regarding claims 7 and 14, Uchiyama discloses that the filling layer is silicon dioxide (col. 9, ln. 64-67).

Regarding claims 8-10, 16-18 and 40, Yu discloses that the shapes and sizes of the patterned portions are variables that may be determined by one of ordinary skill in the art. Specifically, Yu states, "Any suitable spacing between the stripe structures 34a can be used, depending on the process need. The width of the strip structures 34a also depends on what the process requires, such as depending on the width of the trench and so on." (col. 4, ln. 42-54). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine optimal shapes and sizes of the patterned portions of Yu, depending upon the sizes and shapes of the semiconductor devices on the active areas of the wafer and the sizes and shapes of the necessary isolation trenches in the wafer, because such variables of art recognized importance are subject to routine experimentation and discovery of an optimum value for such variables is obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955).

Regarding claim 11, Uchiyama discloses providing a process wafer, forming a nitride mask over the wafer, providing the wafer and mask with active area (CR) trenches and at least one inactive area (DR) trench, forming a filling layer (6) over the active area trenches and the inactive area trenches to substantially fill the trenches, and planarizing the wafer process surface

such that the active area trenches and the inactive area trenches are substantially coplanar (Fig. 8(a)-10(b); col. 9, ln. 31 – col. 10, ln. 8).

Uchiyama does not disclose forming a patterned resist layer between the active and inactive trenches and removing the filling layer not covered by the resist layer. Like Uchiyama, Yu discloses forming isolation trenches in a semiconductor substrate, wherein isolation filling material is deposited into the trenches and then planarized to form coplanar trenches. Yu teaches that when using a planarization method such as that of Uchiyama, the trenches are subjected to undesirable dishing and erosion of the nitride mask layer (col. 1, ln. 31-53). To avoid the problems with the planarization method used by Uchiyama and the conventional prior art, Yu suggests forming a resist layer including first patterned portions overlying the active area, an unpatterned portion overlying the trenches, and lithographically patterning the resist layer to form second patterned portions overlying the substrate in between the trenches, removing the filling layer portions not covered by the resist layer, removing the resist layer and planarizing the wafer surface (col. 4, ln. 15-37). By forming the second patterned portions to form a dummy structure between the trenches, Yu discloses that the etching rate of all areas of the filling layer can be made uniform, thus preventing the dishing and nitride mask erosion problems of the prior art. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method of Yu, including the steps of forming a resist layer including patterned portions disposed between the trenches and removing the filling layer portions not covered by the resist layer, in the isolation planarization process of Uchiyama because Yu teaches that this method can successfully prevent the dishing and mask erosion problems inherent in the prior art.

Uchiyama does not disclose that the inactive area trenches overlie a laser-marked portion. Applicant's admitted prior art discloses that it is conventional in the art to form a laser-marked identification mark on the periphery of a wafer so as to be able to track the wafer throughout the various processing steps that it will undergo (paragraph 002). At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide a laser-marked identification mark at the inactive peripheral area of the wafer of Uchiyama in order to be able to track each particular wafer through its processing steps.

Regarding claim 15, Yu discloses that the first patterned portions are a reverse tone mask (col. 4, ln. 15-16).

Regarding claim 20, the admitted prior art discloses that the practice in industry is to add a laser mark of readable information consisting of alphanumeric characters or barcodes to the wafer (pg. 1, para. 002).

Regarding claims 33 and 36, Uchiyama discloses providing a process wafer, forming a nitride mask over the wafer, providing the wafer and mask with active area (CR) trenches and at least one inactive area (DR) trench, forming a filling layer (6) over the active area trenches and the inactive area trenches to substantially fill the trenches, and planarizing the wafer process surface such that the active area trenches and the inactive area trenches are substantially coplanar (Fig. 8(a)-10(b); col. 9, ln. 31 – col. 10, ln. 8).

Uchiyama does not disclose forming a patterned resist layer between the active and inactive trenches and removing the filling layer not covered by the resist layer. Like Uchiyama, Yu discloses forming isolation trenches in a semiconductor substrate, wherein isolation filling material is deposited into the trenches and then planarized to form coplanar trenches. Yu teaches

that when using a planarization method such as that of Uchiyama, the trenches are subjected to undesirable dishing and erosion of the nitride mask layer (col. 1, ln. 31-53). To avoid the problems with the planarization method used by Uchiyama and the conventional prior art, Yu suggests forming a resist layer including patterned portions disposed between the trenches and removing the filling layer portions not covered by the resist layer (col. 4, ln. 15-37). By this method, Yu discloses that the etching rate of all areas of the filling layer can be made uniform, thus preventing the dishing and nitride mask erosion problems of the prior art. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method of Yu, including the steps of forming a resist layer including patterned portions disposed between the trenches and removing the filling layer portions not covered by the resist layer, in the isolation planarization process of Uchiyama because Yu teaches that this method can successfully prevent the dishing and mask erosion problems inherent in the prior art.

Uchiyama does not disclose that the inactive area trenches overlie a laser-marked portion. Applicant's admitted prior art discloses that it is conventional in the art to form a laser-marked identification mark on the periphery of a wafer so as to be able to track the wafer throughout the various processing steps that it will undergo (paragraph 002). At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide a laser-marked identification mark at the inactive peripheral area of the wafer of Uchiyama in order to be able to track each particular wafer through its processing steps.

Yu discloses that the shapes and sizes of the patterned portions are variables that may be determined by one of ordinary skill in the art. Specifically, Yu states, "Any suitable spacing between the stripe structures 34a can be used, depending on the process need. The width of the

strip structures 34a also depends on what the process requires, such as depending on the width of the trench and so on." (col. 4, ln. 42-54). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine optimal shapes and sizes of the patterned portions of Yu, depending upon the sizes and shapes of the semiconductor devices on the active areas of the wafer and the sizes and shapes of the necessary isolation trenches in the wafer, because such variables of art recognized importance are subject to routine experimentation and discovery of an optimum value for such variables is obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955).

Regarding claim 37, Uchiyama discloses providing a process wafer, forming a nitride mask over the wafer, providing the wafer and mask with active area (CR) trenches and at least one inactive area (DR) trench, forming a filling layer (6) over the active area trenches and the inactive area trenches to substantially fill the trenches, and planarizing the wafer process surface such that the active area trenches and the inactive area trenches are substantially coplanar (Fig. 8(a)-10(b); col. 9, ln. 31 – col. 10, ln. 8).

Uchiyama does not disclose forming a patterned resist layer between the active and inactive trenches and removing the filling layer not covered by the resist layer. Like Uchiyama, Yu discloses forming isolation trenches in a semiconductor substrate, wherein isolation filling material is deposited into the trenches and then planarized to form coplanar trenches. Yu teaches that when using a planarization method such as that of Uchiyama, the trenches are subjected to undesirable dishing and erosion of the nitride mask layer (col. 1, ln. 31-53). To avoid the problems with the planarization method used by Uchiyama and the conventional prior art, Yu suggests forming a resist layer including first patterned portions overlying the active area, an

unpatterned portion overlying the trenches, and second patterned portions overlying the substrate in between the trenches, removing the filling layer portions not covered by the resist layer, removing the resist layer and planarizing the wafer surface (col. 4, ln. 15-37). By forming the second patterned portions to form a dummy structure between the trenches, Yu discloses that the etching rate of all areas of the filling layer can be made uniform, thus preventing the dishing and nitride mask erosion problems of the prior art. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method of Yu, including the steps of forming a resist layer including patterned portions disposed between the trenches and removing the filling layer portions not covered by the resist layer, in the isolation planarization process of Uchiyama because Yu teaches that this method can successfully prevent the dishing and mask erosion problems inherent in the prior art.

Uchiyama does not disclose that the inactive area trenches overlie a laser-marked portion. Applicant's admitted prior art discloses that it is conventional in the art to form a laser-marked identification mark on the periphery of a wafer so as to be able to track the wafer throughout the various processing steps that it will undergo (paragraph 002). At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide a laser-marked identification mark at the inactive peripheral area of the wafer of Uchiyama in order to be able to track each particular wafer through its processing steps.

Response to Arguments

The Examiner agrees with Applicant's argument that Iwamatsu does not disclose planarizing the process surface such that the active area trenches and inactive area trenches are co-planar. Therefore those rejections have been withdrawn.

Allowable Subject Matter

Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for the indication of the allowable subject matter of claim 19 is the inclusion therein, in combination as currently claimed, of the limitation of patterning the first patterned portions and second patterned portions of the resist using two separate masks. This limitation is found in claim 19 and is neither disclosed nor taught by the prior art of record, alone or in combination.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
April 26, 2006

Zandra V. Smith
Supervisory Patent Examiner

Zandra V. Smith
Supervisory Patent Examiner
5/1/2006